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(71) Applicants
Visage Inc (USA-Massachusetts)
12 Michigan Avenue, Natick, Massachusetts 01760, United States of America

(72) Inventor
Jerry Roberts

(74) Agent and/or Address for Service
John Orchard & Co., Staple Inn Buildings North, High Holborn, London WC1V 7PZ

(54) Synchronizing video sources

(57) A video overlay controller accepts video inputs from diverse sources such as video disk players, video tape players, computer video generators, and the like, and provides synchronizing signals which stably lock the video sources to each other for simultaneous display. Synchronization is achieved within eight field times at most. Both interlaced and non-interlaced sources may be mixed for display.

Color graphics adapter 12 is synchronized with a video disk player 10 by control of clock pulses provided by an oscillator 124 to the adapter for setting its operating frequency. The clock pulse frequency is controlled (i) in a horizontal sync section 102 wherein the oscillator 124 is controlled by a phase comparator 122 receiving the adapter horizontal sync signal CGAHSYNC and a horizontal reference signal HREF; (ii) in a vertical sync section 100 wherein the oscillator output can be so gated as to halve the effective frequency if the adapter vertical sync signal CGAVSYNC is detected as having more than a certain misalignment (one-half scan line) with the disk vertical sync signal NTSCVSYNC.

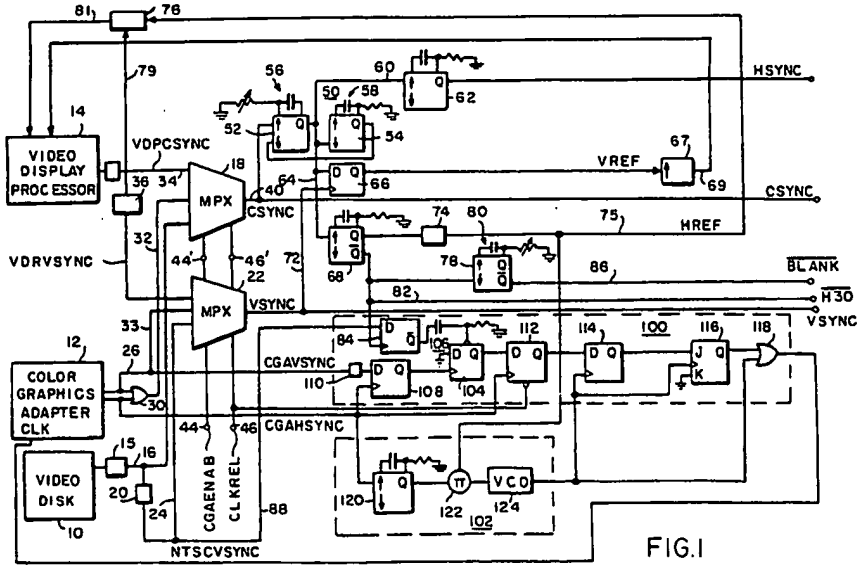

FIG.1

GB 2 175 470 A

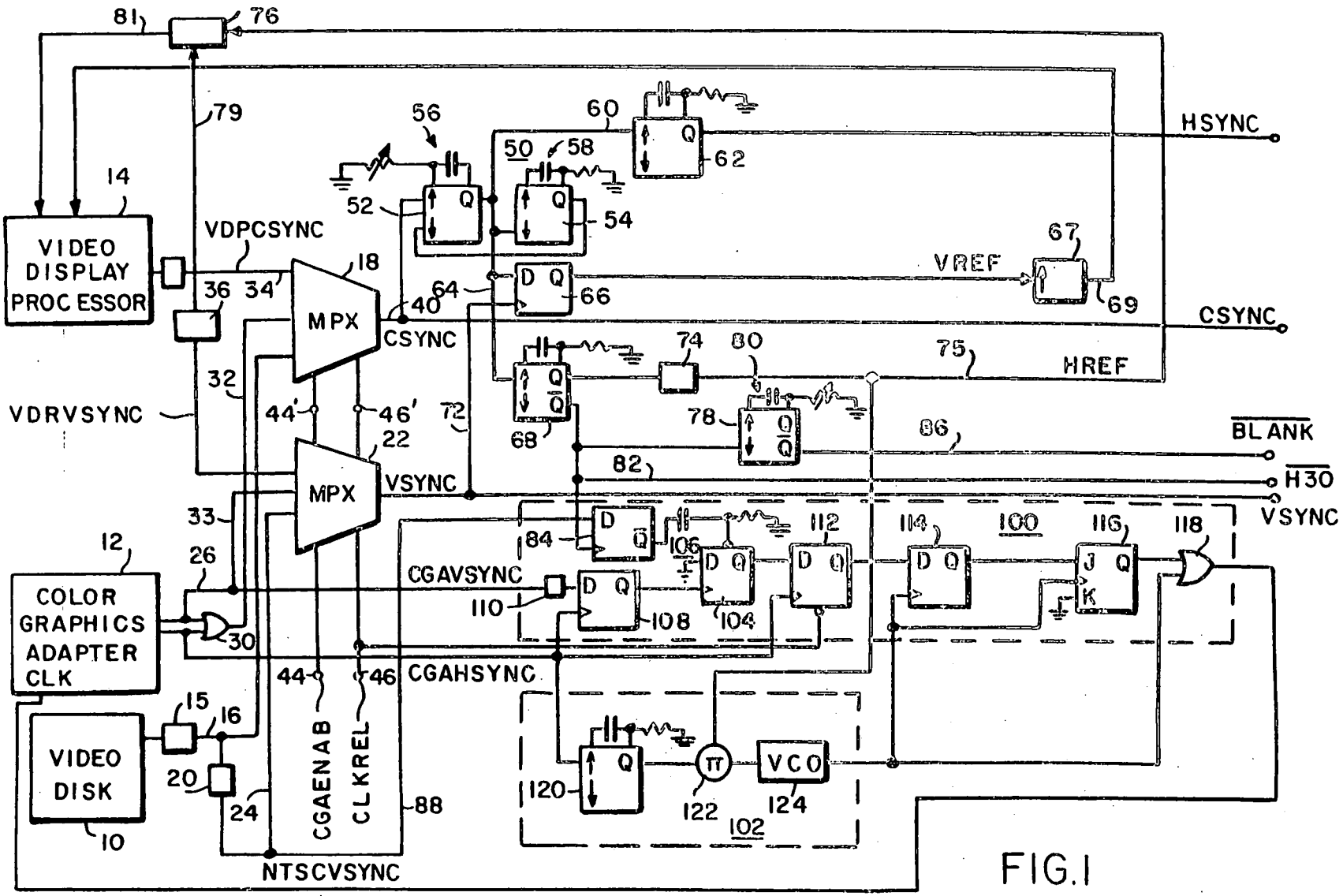

FIG.1

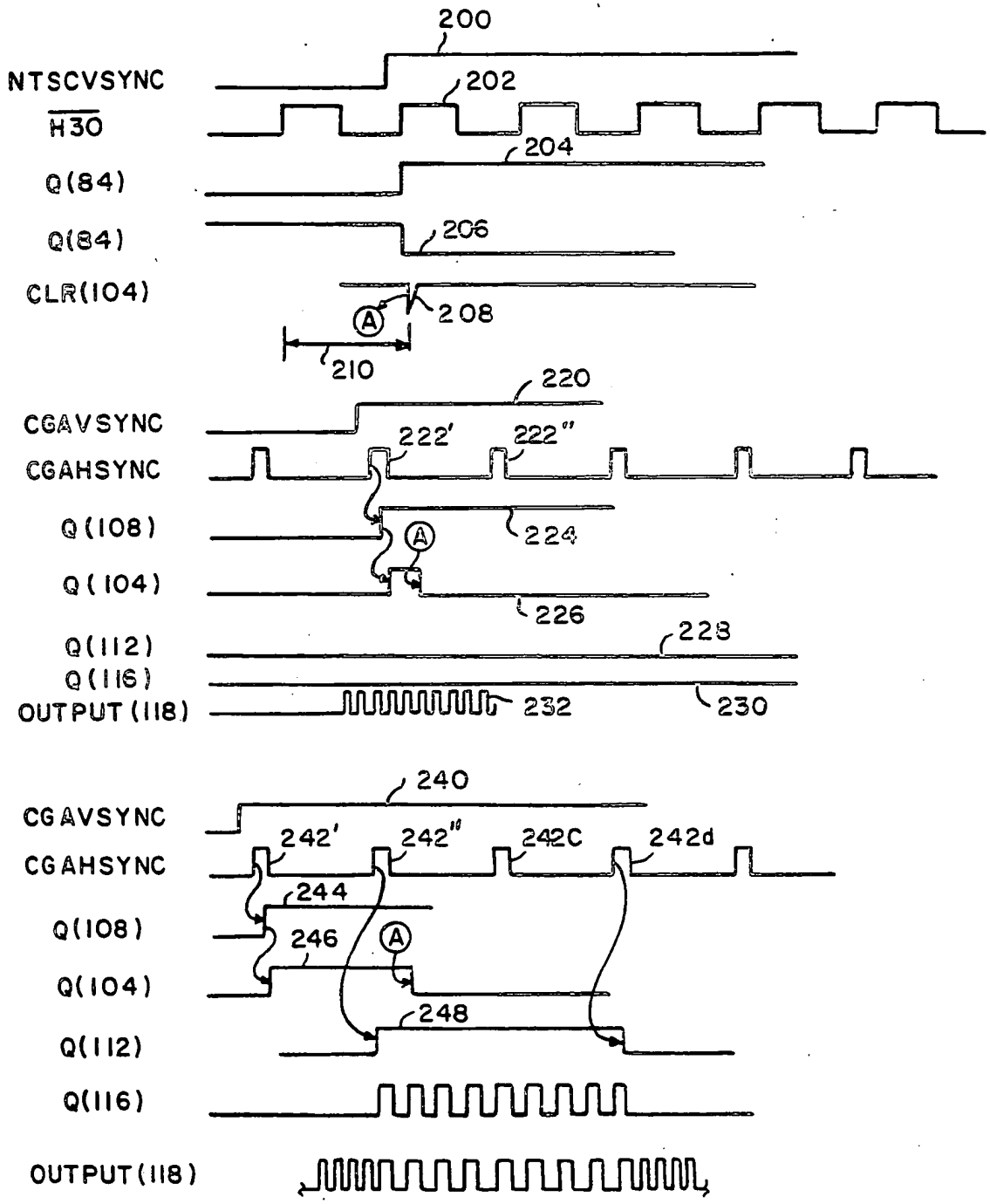
200
NTSCVSYNC
202
H30
204
Q(84)
Q(84)
206
CLR(104)
A
208
210
220
CGAVSYNC
222'
222"
CGAHSYNC
Q(108)
A
224
Q(104)
226
228
Q(112)
Q(116)
OUTPUT(118)
232
230
240
CGAVSYNC
242'
242"
242C
242d
CGAHSYNC
244
Q(108)
246
A
Q(104)
248
Q(112)
Q(116)
OUTPUT(118)

FIG. 2

SPECIFICATION

Video overlay controller

Background of the Invention

A. Field of the Invention

The invention related to video overlay controllers and, more particularly, to apparatus for synchronizing the video signal from separate video sources.

B. Prior Art

Video overlay controllers control the simultaneous display ("overlay") of video signals from two or more sources. An important characteristic of such controllers is the synchronization of the video signals from the separate sources so that the resultant composite display provides a stable picture to the viewer.

One technique for providing such synchronization is described in U.S. Pat. No. 4,346,407, issued Aug. 24, 1982 to R. H. Baer. In the circuit of that patent, separate synchronizing loops are provided for establishing frequency and phase coherence between the signals to be synchronized. With this arrangement, long waiting times (up to over 900 field periods or 15 seconds) can be required in order to establish synchronization. Further, the sources to be synchronized must be of the same scan type, i.e., both interlace or both non-interlaced.

Brief Summary of the Invention

A. Objects of the Invention

Accordingly, it is an object of the invention to provide an improved video overlay controller.

Further, it is an object of the invention to provide a video overlay controller that rapidly achieves synchronization between two or more video sources that are to be overlaid.

Yet another object of the invention is to provide a video overlay controller that is operable with video sources of different scan types.

B. Brief Summary of the Invention

In accordance with the present invention, a video overlay controller synchronizes a local source of video, such as computer-generated video, with an external video source, such as a video disk, by separately locking the vertical and horizontal synchronizing signals of one source (e.g. the local source) to the corresponding signals of the other source (e.g. the external source) in such a manner as to achieve both horizontal and vertical synchronization essentially simultaneously and independently, and within no more than eight field times (i.e., approximately 1/7 second) at most. When the two video sources are then overlaid on a video display for simultaneous display, the resultant composite image is highly stable both vertically and horizontally.

Vertical synchronizing circuitry measures the time of occurrence of the vertical synchronizing signals of the local source with respect to that of the external source and, if the difference exceeds a defined amount (specifically, one-half the duration of a horizontal scan), activates scan correction circuitry which brings the time difference to within one-half the horizontal scan time. Horizontal correction circuitry simultaneously reduces errors of less than one-half scan time essentially to zero. The horizontal and vertical synchronization are accomplished in a manner that is essentially independent of each other. Thus, once vertical synchronization is achieved, continued operation to achieve horizontal synchronization does not interfere with or otherwise affect the vertical synchronization.

The controller of the present invention accepts inputs from an external source such as a video disk player, tape player, computer video generator, or the like, as well as from one or more internal video sources such as a video display controller or a color graphics adapter. The scanning format of the sources may differ. Thus, video disk players typically provide outputs in accordance with NTSC standards; these provide for interlaced scanning. Video display processors may accomodate either interlaced or non-interlaced scanning, while color graphics adapters, such as the IBM Color Graphics Adapter, typically provides non-interlaced scan. In the present invention, because of the manner in which synchronization is achieved, both types of sources may be mixed without special precautions.

Detailed Description of the Invention

The foregoing and other and further objects of the invention will be more readily understood from the following detailed description of the invention, when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block and line diagram of a video overlay controller in accordance with the present invention; and

Fig. 2 is a sequence of timing waveforms illustrating the operation of the circuit of Fig. 1 in achieving synchronization.

In Fig. 1, a synchronizing circuit in accordance with the present invention receives inputs from three sources, namely, a video disk player 10, a color graphics adapter 12, and a video display chip 14. The video disk 10 provides as output a standard (NTSC) composite video signal including both video and synchronizing components. The composite (vertical and horizontal) synchronizing signals are separated in a sync separator 15, and the resultant composite sunchronizing signal (NTSCCYYNC) is fed via a lead 16 to a multiplexer 18. This signal typically is adapted for an interlaced scan. In contrast, the color graphics adapter (e.g., a standard IBM Color Graphics Adapter) may utilize a non-interlaced scan. Despite this difference in the characteristics of the signals, the circuit of the present invention readily accomodates these diverse sources to provide a clock signal for the computer-generated graphic display that is synchronized with the particular source that is selected for the external graphics.

A vertical synchronizing signal (NTSCVSYNC) is derived in a known manner from the composite signal via a circuit 20 that may simply comprise an integrator followed by a Schmitt trigger; the resultant is applied to a multiplexer 22 via a lead 24. The color graphics adapter 12 provides a vertical synchronizing signal

(CGAVSYNC) on a lead 26, and a horizontal synchronizing signal (CGAHSYNC) on a lead 28. These signals are applied to multiplexer 18 via an OR gate 30 (which combines them to form a composite synchronizing signal) and a lead 32, and to multiplexer 22 via a lead 33. Finally, the video display processor 14 provides a composite synchronizing signal on a lead 34 which is applied directly as an input to the multiplexer 18. A vertical synchronizing signal VDPVSYNC is derived from the composite signal via an integrator 36 and is applied to the multiplexer 22 via a lead 38.

Multiplexers 18 and 22 each select one of the inputs applied to them and provide the selected inputs as outputs on leads 40, 42, respectively. The selection is performed in accordance with the state of switching inputs CGAENABLE and CLKREL applied to control terminals 44, 44' and 46, 46', respectively. These signals select output from the video disk, the colour graphics adapter, or the video display controller for overlay with respect to each other. The output of multiplexer 18, which is applied to lead 40, is a composite synchronizing signal derived from one of the sources, while the output of multiplexer 22, which is applied to lead 42, is a vertical synchronizing signal selected from the same source.

The output of multiplexer 22 is applied to a missing pulse detector 50 which comprises first and second monostable multivibrators 52, 54 ("one-shots"), respectively. The normal (Q) output of multivibrator 52 is coupled to the negative transition input of multivibrator 54. The normal (Q) output of multivibrator 54 is fed back to the negative transition input of multivibrator 52. RC timing networks 56, 58 control the duration of the output pulses of the multivibrators 52, 54, respectively.

The multivibrators 52 and 54 respond to positive transitions in the input driving signal to provide outputs of controlled duration. The duration of the respective outputs of the multivibrators 52/54 is such that the trailing edge of the output of multivibrator 54 normally coincides in time with the leading edge of the positive-going input to multivibrator 52. When this is the case, the multivibrator 52 is triggered at both its inputs at the same time, and the second input (from multivibrator 54) is redundant, although harmless. If, however, the input to the positive transition input is missing from the input pulse train (due, for example, to the absence of serrations marking the horizontal pulses embedded within the composite synchronizing pulse), the trailing edge of the output of multivibrator 54 triggers the multivibrator 52 at the time it would have been triggered had the input signal been a standard composite synchronizing signal. Multivibrator 52 then provides an output pulse at the appropriate time, despite the absence of the normal input pulse.

The resultant output is then coupled via a lead 60 to a monostable multivibrator 62 which provides an output of precisely defined duration for use as the horizontal synchronizing pulse in the video display device. It is also applied via a lead 64 to the input of a flip-flop 66, as well as to the positive transition input of a monostable multivibrator 68 whose output pulse duration is set by an RC circuit 70 to provide a pulse having a 50% duty cycle at the horizontal line frequency. Flip-flop 66 is clocked from the output of multipolexer 22 on lead 42. The output of flip-flop 66 comprises a vertical reference pulse (VREF) which triggers a monostable multivibrator 67 to form a vertical reset pulse which is applied to the processor 14 via a lead.

The non-inverting (Q) output of multivibrator 68 is passed through a delay 74 which horizontally aligns the raster with the overlay, and is then applied via a lead 75 to a phase comparator 76. Comparator 76 receives a second input comprising the video display processor composite sync signal VDPCSYNC from processor 14 via a lead 77, and supplied an output to processor 14 via a lead 81 for use as a horizontal reference signal by the processor to lock its horizontal frequency output to HREF. The inverting output of multivibrator 68 is applied to the negative transition input of a monostable multivibrator 78 having an RC network 80 for setting the time constant of the resultant pulse, as well as to a lead 82 for use as a horizontal gating signal (H30) and to the clock input of a D-type flip-flop 84. The output of multivibrator 78 is applied to a lead 86 for use as a horizontal blanking signal.

In accordance with the present invention, vertical and horizontal synchronization of the computer-generated display (which is controlled by either the color graphics adapter or by the video display processor) is attained for the color graphics adapter by means of two separate and essentially non-interacting control sections, namely, a vertical sync section 100 and a horizontal sync section 102, and for the video display processor by the HREF and VREF signals described above. The section 100 includes the flip-flop 84 which resets a flip-flop 104 through a differentiator 106. Flip-flop 104 is clocked from a flip-flop 108 which receives a data (D) input comprising the vertical sync signal CGAVSYNC from the color graphics adapter 12 via lead 26 and a delay circuit 110. Flip-flop 108 is clocked by the horizontal sync signal CGAHSYNC from adapter 12 via lead 28. The output of flip-flip 104 derives the data (D) input of a flip-flop 112 which also is clocked by the horizontal sync signal CGAHSYNC from adapter 12 and is reset by the clock release signal CLKREL.

As will shortly be seen below, the output of flip-flop 112 is a pulse whose duration is a measure of the misalignment between the vertical synchronizing signal NTSCVSYNC of the disk 10 and that of the adapter 12 (CGAVSYNC). This pulse is applied to a flip-flop 114 whose output in turn is applied to a J-K flip-flop 116 which derives an OR gate 118. Flip-flops 114 and 116 are clocked from the output of the horizontal synchronizing section 102 which is formed from a monostable multivibrator 120, a phase comparator 122, and a voltage controlled oscillator 124. Multivibrator 120 is triggered from the horizontal synchronizing signal CGAHSYNC which is applied to its positive-transition input, and applies its output to phase comparator 122. The latter also receives an input comprising the horizontal reference signal HREF from lead 76. The difference between these signals drives oscillator 124. The output of oscillator 124 is also applied through the gate 118, together with the output of flip-flop 116. The resultant output of 118 is applied via a lead 126 to the clock input (CLK) of the

color graphics adapter to set the fundamental operating frequency of the latter.

Turning now to fig. 2, the achievement of vertical synchronization will now be described in detail. Assume that computer generated video (whose display is to be controlled by the color graphics adapter 12) is to be overlaid on the output of the disk 10. In that case, the multiplexers 18 and 22 are enabled to select their inputs from the disk 10. The composite synchronizing signal (NTSCCSYNC) from the disk 10 is then used to derive the horizontal synchronizing signal 202 (H30) via the missing pulse detector 50 and flip-flop 68. The first horizontal pulse 202 after the vertical pulse 200 (NTSCVSYNC) triggers multivibrator 84 which then provides an output pulse 204 at its Q output, and the inverse 206 at its complementary output Q. The leading edge of pulse 206 is differentiated in differentiator 106 to form a trigger 208 which resets flip-flop 104. Pulse 208 forms the end of a "window" 210 which extends for one-half the horizontal sync period on either side of the preceeding horizontal synchronizing pulse embedded in NTSCCSYNC.

Assume now that the operation of the adapter 12 is such that its vertical synchronizing signal 220 (CGAVSYNC) occurs at the time shown in Fig. 2 in relation to the disk vertical synchronizing signal 200; thus, it falls within a half-scan line of the video vertical synchronizing signal, NTSCVSYNS. Note that this lies within the "window" 210. (The leading edge of the horizontal synchronizing signal (CGAHSYNC) of the adapter is slightly displaced from alignment with that of the vertical signal in order to avoid ambiguity when the horizontal signal is used to clock the vertical signal in the flip-flop 108). The first horizontal signal 222' occurring after the vertical signal 220 sets flip-flop 108. The output 224 of this flip-flop in turn triggers flip-flop 104. The latter remains "set" until the arrival of the reset pulse 208 from flip-flop 84. The resultant output of flip-flop 104 is shown at 226 in Fig. 2. The output (226) of flip-flop 104 is applied as input to flip-flop 112 but fails to set this flip-flop since it terminates before the subsequent clock input 222 to the flip-flop 112. Thus, the output of flip-flop 112 remains at the "low" or "reset" level as shown at 228 in Fig. 2. Accordingly, flip-flop 114 remains reset, as does flip-flop 116 whose output is shown at 230 in Fig. 2. The output of OR gate 118 is then supplied solely by oscillator 124 as shown at 232 in Fig. 2.

Now assume that the vertical synchronizing signal CGAVSYNC occurs at an earlier time as shown at 240 in Fig. 2. At the first horizontal synchronizing signal CGAHSYNC (shown at 242' in Fig. 2) following the vertical signal, flip-flop 108 is set (signal 244, Fig. 2) and flip-flop 104 is then set (246, Fig. 2) from flip-flop 108. As was previously the case, flip-flop 104 is reset by the pulse 208. However, prior to this reset, the horizontal pulse 242" sets flip-flop 112 (waveform 248, Fig. 2) from flip-flop 104 as shown at 248 in Fig. 2. This in turn sets flip-flop 114 and then flip-flop 116 (waveform 250, Fig. 2) on the next clock pulse from oscillator 124. Flip-flop 116 then toggles between the "set" and "reset" states in response to successive clocking signal from the oscillator 124.

When in the "set" state, the output of flip-flop 116, when applied to gate 118, effectively masks the output of oscillator 124, as shown at 252 in Fig. 2. When reset, it allows the oscillator output to pass through the gate without interference. Thus, the effective output of gate 118 (waveform 252, Fig. 2) is a clock signal that is at one-half the frequency of the oscillator output as long as flip-flop 114 is set. Accordingly, the next horizontal synchronizing pulse, which would normally occur at 242c as shown in Fig. 2, is delayed and occurs instead at the time shown at 242d. When it does occur, it terminates the output of flip-flop 112 and thus of flip-flops 114 and 116. Accordingly, the output of oscillator 124 passes through gate 118 without interruption, and thus at its normal rate. The phase misalignment of the adapter vertical synchronizing signal with respect to the disk vertical synchronizing signal is thus effectively halved during each field time, until it is brought within one half scan line of the disk synchronizing signal, at which time further correction is made by the horizontal correction circuitry only. In this manner, vertical synchronization is rapidly achieved, and within no more than eight field times, at most (since eight halvings are the maximum required to cover a phase misalignment of one full field). Further, it is accomplished essentially independently of the horizontal synchronization, since vertical phase correction is accomplished using only full multiples of scan lines. Thus, horizontal phase correction can proceed concurrent with vertical phase correction, and the time required to achieve synchronization is thereby further reduced. Further, the shift in the effective clock rate in the vertical circuitry during vertical phase correction serves to accommodate the non-interlaced color graphics adapter to the interlaced video disk output, and interlaced and non-interlaced sources are thus handled by the circuit of the present invention.

Returning now to the horizontal synchronizing section 102 in Fig. 1, the oscillator 124 provides the basic timing frequency for the adapter 12, as previously noted. In one physical embodiment of the present invention, this oscillator was set to operate at a frequency of 14.34965 megahertz. The instantaneous frequency of the oscillator is established by the output of phase comparator 122 which in turn is dependent on the difference between the time of occurrence of the horizontal synchronizing signal CGAHYNC as applied to junction 122 via the one-shot 120, and the horizontal reference signal HREF. Any time difference between these signals causes the oscillator 123 to speed up or slow down as appropriate and thus bring the two signals into synchronization. Thus, both vertical and horizontal synchronization are rapidly achieved, and in a manner that is essentially independent of each other.

CONCLUSION

From the foregoing it will be seen that I have provided an improved video overlay controller. The controller synchronizing signals that locks the diverse sources to each other within at most eight display field times to provide an unusually stable display. Both interlaced and non-interlaced sources may be mixed for display.

CLAIMS

1. A video display controller, comprising:

A. means for receiving primary and secondary

video signals containing horizontal and vertical synchronizing signals for controlling a raster scan display,

B. means for forming from said primary video signal a primary reference signal synchronized with said primary horizontal synchronizing signal and occurring in specified relation to said primary vertical synchronizing signal,

C. means for forming from said secondary video signal a secondary reference signal synchronized with said secondary horizontal reference signal and occurring in specified relation to said secondary vertical synchronizing signal, and

D. controlling means selectively responsive to said primary and secondary reference signals for controlling the instantaneous rate at which said secondary synchronizing signals are generated.

2. A video display controller according to claim 1 in which the means for forming said primary reference signal comprises means responsive to the occurrence of a primary horizontal horizontal synchronizing signal subsequent to the occurence of a primary vertical synchronizing signal.

3. A video display controller according to claim 1 in which said controlling means responds to said primary and secondary reference signals only when the time difference therebetween is greater than a predefined amount.

4. A video display controller according to claim 1 in which said controlling means responds to said primary and secondary reference signals only when the time difference therebetween is greater than the time of approximately one-half horizontal scan line.

5. A video display controller according to claim 1 in which said controlling means comprises

(1) an oscillator for supplying timing pulses to a master clock from which the timing relationships of said secondary synchronizing signals are derived, and

(2) means responsive to said primary and secondary reference signals for generating a gating signal whose duration is indicative of the time difference between said reference signals,

(3) means responsive to said gating signal for selectively limiting the application of said timing pulses to said clock when said gating exceeds a predetermined duration.

6. A video display controller according to claim 1 in which said controlling means includes means for adjusting the vertical phase of said secondary video signal by integral numbers of scan lines.

7. A video display controller according to claim 6 in which said controlling means further includes means for generating secondary horizontal synchronizing signals concurrent with secondary vertical synchronizing signals to thereby concurrently provide vertical and horizontal synchronization.

8. A video display controller, comprising

A. means for extracting vertical and horizontal synchronizing signals from a first video source that is to serve as a master source,

B. means including a controllable clock generator for generating vertical and horizontal synchronizing signals for controlling the display of a second video source synchronously with said first source,

C. means for generating a first signal indicative of the misalignment of the vertical synchronizing signal of said second source with respect to that of said first source, and

D. means forming a vertical correction circuit responsive to said first signal for applying vertical correction signals to said clock only when said first signal exceeds a predetermined amount.

9. A video display controller substantially as described herein with reference to the accompanying drawings.

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